

TEST CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT  
EFFECTIVELY CARRYING OUT VERIFICATION OF  
CONNECTION OF NODES

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ABSTRACT OF THE DISCLOSURE

10        A test circuit is incorporated in a device having an output circuit for outputting a signal, and the test circuit carries out a verification of a connection of nodes of the device. The test circuit has a test data generating circuit and a test output buffer connected in parallel with output nodes of the output circuit. The test data generating circuit generates test data for carrying out a verification of a connection of the output nodes, and the test output buffer receives test data from the test data generating circuit and outputs the test data to the output nodes. Similarly, a test circuit is incorporated in a device having an input circuit for inputting a signal, and the test circuit carries out a verification of a connection of nodes of the device. The test circuit has a test data generating circuit and a test input buffer connected in parallel with input nodes of the input circuit. The test data generating circuit generates test data for carrying out a verification of a connection of the input nodes, and the test input buffer receives test data from the test data generating circuit and inputs the test data to the input nodes.

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